REMARKS

The Examiner's Office Action of November 13, 2003has been received and carefully reviewed. Claims 1 and 3-12 have been amended, no claims have been cancelled or added. Therefore, claims 1-12 are pending in this application. For at least the following reasons, it is respectfully submitted that this application is in condition for allowance.

First of all, claims 7-12 are allowable over the prior art of record, but are objected because of informalities of grammatical error. Since claims 7-12 are amended in compliant with the examiner's suggestion described in the Action, the objection to the claims 7-12 is no longer applicable. Further, claims 1-6 are also objected by the same reason as applied to claims 7-12. Since claims 1-6 are also amended in compliant with the examiner's suggestion described in the Action, the objection to the claims 1-6 is no longer applicable. These amendments are made to correct the grammatical errors so that no claim narrows its scope by this amendment.

In the Action, claims 1-6 are rejected under 35 U.S.C. 102(b) as being unpatentable over Hubbins. The invention defined in independent claim 1 relates to a memory control circuit, specifically the first embodiment. The characteristics of the invention claimed in claim 1 are,

(a) **a watching circuit**, which receives the first and second processing request signals, the watching circuit observing, based on these signals,

whether the first and second processing devices request access to the memory, and

(b) **a control circuit** generating the selection signal, the control circuit outputting the selection signal for selecting the first address signal prior to the second address signal when the observations of the watching circuit indicates that both of the first and second processing devices request access to the memory.

According to this structure, The control circuit (corresponding to an inverter 106, an OR gate 107, an AND gate 108 and a NOR gate 109 in Fig. 1) outputs an enable signal (corresponding to a signal F1 in Fig. 1) to let a memory be enable. Specifically, under the following two conditions (at least the second condition is important), the enable signal has a voltage level, which designates the memory to be enabled.

(1) At the time that the first or second processing request signals(corresponding to a signal CWE or a signal ERE in Fig. 1) has a voltage level for requesting access to the memory

(2) During a period that a signal from the watching circuit (corresponding to a signal B1 in Fig. 1) as a result of watching has a voltage level that both of the first and second processing devices request access to the memory (that is, the period that F1 has an L level during the time t2-t3 in Fig. 2).

Specifically, it is important for the invention to control the voltage level of the enable signal during the period above-described in (2).

According to the structure having the characteristics described above in (1) and (2), it is possible to extend the condition substantially by the signal from the watching circuit as a result of watching that the enable signal maintains its voltage level designating the memory to be enable only for the period that both of the first and second processing devices have a voltage level for requesting access to the memory. In other words, during the time t2 in Fig. 2, after the first and second processing request signals become the L level, it is possible to maintain the voltage level of the enable signal at the L level. Thus, even if the first processing request signal comes in first, it is possible to perform the process based on the second processing request signal in the condition that the memory is enabled during the substantially extended period described above, without invalidating the second processing request signal.

On the other hand, Hubbins discloses the multiprocessor interface device having an arbitration latch 16. In order to access A RAM 1, one of a port A an a port B is selected by the signal ACTA or ACTB outputted from the arbitration latch 16. However, Hubbins does not disclose how to control the multiprocessor interface device when both of the port A and port B request access to the RAM 1. Specifically, Hubbins does not disclose that the control circuit controls the enable signal in response to the result of the watching circuit, as claimed in claim 1. Thus, the any circuits disclosed in Hubbins can not perform the above-described operation of the invention.

Therefore, since Hubbins does not disclose or suggest the claimed memory control circuit having the characteristics (a) and (b) described above, claim 1 clearly is not anticipated by Hubbins, and is deemed to be clearly

patentable over Hubbins, and the rejection of claim 1 accordingly should be withdrawn.

Further, claims 2-6 depend from claim 1 directly or indirectly. Since Applicants believes that claim 1 includes a patentable subject matter, the rejection of claims 2-6depended from claim 1 should be withdrawn.

In the Action, claims 1-6 are rejected under 35 U.S.C. 102(e) as being unpatentable over Duranton. Duranton discloses that a memory system includes a unit COMP. When there is a conflict in a single memory that operations of writing and reading are enabled simultaneously, the unit detect the conflict by comparing some of bits of the 8-bit word MC_W with some of bits of the 8-bit word MC_R. However, Duranton simply suggest one of the operations is prioritized over another to resolve the conflicting problem. Thus, Duranton does not disclose the control of the invention that even if the first processing request signal comes in first, it is possible to perform the process based on the second processing request signal in the condition that the memory is enabled during the substantially extended period described above, without invalidating the second processing request signal. Accordingly, Duranton does not disclose that the control circuit controls the enable signal in response to the result of the watching circuit, as claimed in claim 1. Thus, the any circuits disclosed in Duranton can not perform the above-described operation of the invention.

Therefore, since Duranton does not disclose or suggest the claimed memory control circuit having the characteristics (a) and (b) described above, claim 1 clearly is not anticipated by Duranton, and is deemed to be clearly

patentable over Duranton, and the rejection of claim 1 accordingly should be withdrawn.

Further, claims 2-6 depend from claim 1 directly or indirectly. Since Applicants believes that claim 1 includes a patentable subject matter, the rejection of claims 2-6depended from claim 1 should be withdrawn.

It is noted that this Amendment has been prepared using the requested new format. If there are any irregularities in this format, it would be greatly appreciated if Applicant's Counsel would be so advised

In view of the foregoing, the application is deemed to be in condition for allowance and such is earnestly solicited. Should any fee be needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Examination of the application is respectfully requested.

Respectfully submitted,

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